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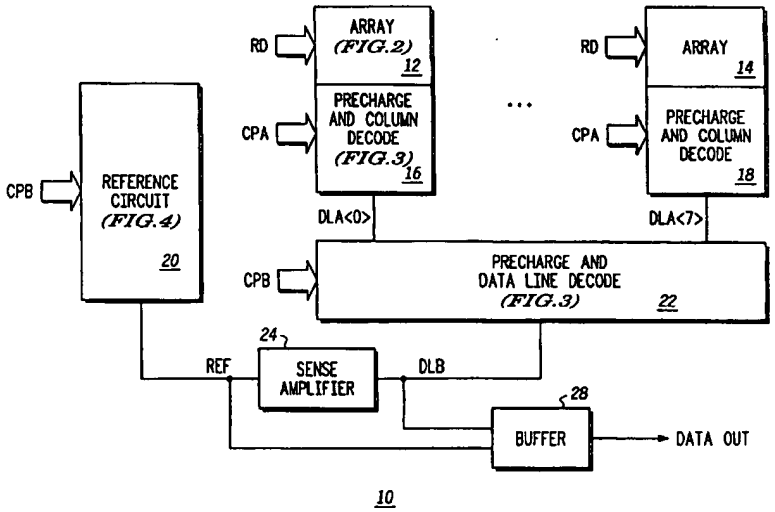
(54) Title: METHOD AND APPARATUS FOR READING AN INTEGRATED CIRCUIT MEMORY



(57) **Abstract:** A memory (10) includes a precharge and decode circuit (16) coupled to each of the bit lines to precharge the bit lines to a predetermined voltage prior to an access. During a read cycle of the memory (10), the precharge transistor (48) is decoupled from only the selected bit line in response to a column decode signal (CPB). The other bit lines remain coupled to the precharge and decode circuit (16). Also, a reference circuit (20) matches the impedance of the data path, and provides a reference current that is about half way between the read current for a logic one and the read current for a logic zero. A data line voltage and a reference voltage results from current flowing into the bit line (BL) and a reference bit line (BLREF) concurrently from a load transistor (124, 126) in a sense amplifier (24) and controlled by a column decode signal (CPB) in the precharge and data line decode circuit (22).

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METHOD AND APPARATUS FOR READING AN INTEGRATED CIRCUIT MEMORY

Field of the Invention

This invention relates generally to integrated circuit memories, and more particularly to a memory having a low power read cycle.

Related Art

With today's information systems, it is preferable to minimize the power consumed by a memory device utilized in the information system. A low power memory device is especially desirable in battery powered systems or systems susceptible to over heating. Another desirable feature for memory devices is reduced access time. Reducing the access time of a memory device enables a system utilizing the memory device to operate at faster speeds. What is desirable is a memory device that consumes less power and/or has faster access times.

Brief Description of the Drawings

The present invention is illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings and in which like reference numerals refer to like elements and in which:

FIG. 1 illustrates, in block diagram form, a memory in accordance with the present invention.

FIG. 2 illustrates, in schematic diagram form, a memory array of the memory of FIG. 1.

FIG. 3 illustrates, in schematic diagram form, a portion of the precharge and decode circuits of the memory of FIG. 1.

FIG. 4 illustrates, in schematic diagram form, the reference circuit of the memory of FIG. 1.

FIG. 5 illustrates, in schematic diagram form, the sense amplifier of the memory of FIG. 1.

FIG. 6 illustrates various signals of the memory of FIG. 1 useful for understanding a read operation.

Description of a Preferred Embodiment

Generally, the present invention provides a memory having an array of memory cells coupled to bit lines and word lines. The bit lines are precharged to a predetermined voltage using a precharge decode circuit. During a read cycle of the memory, a column decode signal decouples the precharge and decode circuit from only the selected bit line. The predetermined voltage is maintained on each of the unselected bit lines. A first current source provides a current to the selected bit line through a read data path and a second current source provides a current through a reference line during a read cycle. The read current through the data path is a first value for a stored logic high state and a second value for a stored logic low state. The reference line concurrently sinks a predetermined current that is between the first value and the second value produced by the read data path during a read cycle. Also, the reference line uses dummy elements to match the RC delay of the bit lines of the array. In the illustrated embodiment, the data line current source provides the current through two levels of column decoding, and is the only source of read current through the data path. The reference line current source provides current through one level of column decoding to more precisely match the data path RC delay. A sense amplifier

has a first input coupled to the bit line and a second input coupled to the reference line. A differential voltage is developed on the two sense amplifier inputs by the differing reference line current and data path current that corresponds to the state of a selected memory cell relative to the state of the reference cell.

By decoding the precharge voltage applied to the selected bit line and to the reference line, the data path RC delay can be more accurately matched, thereby providing for faster sensing and better noise margins. By having only one current path during the read cycle, power consumption of the integrated circuit memory is reduced.

FIG. 1 illustrates, in block diagram form, a memory 10 in accordance with the present invention. In the illustrated embodiment, memory 10 is a mask programmable read only memory (ROM). However, in other embodiments, memory 10 may be another memory type. Memory 10 includes a plurality of memory arrays including memory arrays 12 and 14. Precharge and column decode circuit 16 is coupled to memory array 12 and precharge and column decode circuit 18 is coupled to memory array 14. Precharge and column decode circuits 16 and 18 function to both control bit line precharge and the coupling of a bit line to precharge and data line decode 22 in response to a column decode signal CPA via a data line labeled DLA<0> or DLA<7>, respectively. Note that although two memory arrays are illustrated in FIG. 1, more memory arrays and corresponding precharge and column decode circuits may be present in other embodiments. Precharge and data line decode 22 couples a selected one of the data lines, such as for example, data line DLA<0> to sense amplifier 24 in response to a column decode signal labeled CPB. Note that there are two levels of decode in memory 10. Precharge and column decode circuits 16 and 18 are the first level of decode and precharge and data line decode 22 is a second level of

decode. Reference circuit 20 receives column address signals CPB and provides a reference current REF to sense amplifier 24 during a read cycle of memory 10. Sense amplifier 24 has input/output terminals for receiving reference current REF and a data line current labeled DLB. During a read cycle of memory 10, sense amplifier 24 compares reference current REF to data line current DLB, to determine the logic state of a selected memory location. Buffer 28 is coupled to data line DLB and reference line REF and receives a data signal corresponding to the state of the selected memory location. In response, buffer 28 provides a buffered data out signal labeled DATA OUT. Note that there can be any number of memory arrays in memory 10, for example, in memory 10 there are 8 memory arrays. In another embodiment, there can be more or less than 8 memory arrays.

FIG. 2 illustrates, in schematic diagram form, a representative portion of memory array 12 of memory 10 of FIG. 1. Memory array 12 includes a plurality of word lines, including word lines labeled WL<0> through WL<3>, extending in one direction. A plurality of bit lines, including bit lines labeled BL<0> through BL<7>, extend in another direction across the word lines. Memory array 10 is a mask programmable ROM and a transistor, such as for example transistor 26, is coupled to a word line and a bit line at predetermined intersections of the word lines and bit lines depending on the particular data being stored in memory array 12. In the illustrated embodiment, a transistor is located at address locations that are intended to provide a low logic state corresponding to a logic "0" when read. Locations that do not have a transistor will be read as a high logic state corresponding to a logic "1" when read. By way of example, transistor 26 has a gate coupled to a word line labeled WL<2>, a drain coupled to bit line BL<6>, and a source coupled to V_{SS}. The other transistors are connected to the bit lines and word lines randomly and are not intended to reflect any

particular data. In the illustrated embodiment, V_{SS} is coupled to ground potential and V_{DD} is coupled to a positive supply voltage, such as for example 1.5 volts.

FIG. 3 illustrates, in schematic diagram form, a portion of the precharge and decode circuits of the memory of FIG. 1. FIG. 3 illustrates two levels of column decoding and bit line and data line precharge circuits. A first level of precharge and decode includes column decode transistors 32, 34, 36, 38, 40, 42, 44, and 46 for receiving one of first level column decode signals CPA<0> - CPA<7>, respectively. In addition, the first level column decode signals CPA<0> - CPA<7> are provided to input terminals of inverters 64, 66, 68, 70, 72, 74, 76, and 78, respectively. Each of the bit lines is coupled to a precharge transistor. In the illustrated embodiment, one precharge N-channel transistor of precharge N-channel transistors 48, 50, 52, 54, 56, 58, 60, 62 is coupled to one corresponding bit line of memory array 12 in FIG. 2 in response to a deasserted column decode signal CPA<0> - CPA<7>. For example, precharge transistor 48 has a drain coupled to bit line BL<0>, a gate coupled to an output of inverter 64, and a source coupled to V_{SS}. One of bit lines BL<0> through BL<7> is coupled to data line DLA<0> when a corresponding one of the column decode signals CPA<0> - CPA<7> is asserted. Data line DLA<0> is coupled to data line DLB via transistor 80 in response to column decode signal CPB being asserted. Column decode signal CPB is the second level of column decoding. N-channel decode transistor 80 has a first drain/source terminal connected to data line DLA<0>, a second drain/source terminal connected to data line DLB, and a gate coupled to receive second level column decode signal CPB. Data line precharge tranistor 82 has a drain connected to data line DLA<0>, a gate coupled to the output of inverter 84, and a source connected to V_{SS}. An input terminal of inverter 84 is coupled to receive column decode signal

CPB. Data line DLA<0> is precharged to V_{SS} in response to column decode signal CPB, provided to transistor 82 via inverter 84, being deasserted, or at a logic low. When CPB is asserted as a logic high, precharge transistor 82 is substantially non-conductive, transistor 80 is conductive, and a current representing a data signal from data line DLA<0> is provided to data line DLB. Note that a precharge and decode circuit similar to the two level precharge and decode circuit of FIG. 3 is provided for each array of memory 10. Another second level precharge circuit like that provided by transistors 80 and 82, and inverter 84 is repeated for each additional memory array.

FIG. 4 illustrates, in schematic diagram form, the reference circuit 20 of memory 10 of FIG. 1. Reference circuit 20 includes a plurality of parallel-connected N-channel decode transistors 90, 92, 94, 96, 98, 100, 102, and 104 that receive one of column decode signals CPB<0> through CPB<7>, respectively. Each of the decode transistors 90, 92, 94, 96, 98, 100, 102, and 104 has a drain coupled to an input of sense amplifier 24 labeled REF, a gate for receiving one of column decode signals CPB<0> through CPB<7>, and a source. N-channel transistor 88 has a drain connected to the source terminals of the parallel-connected N-channel transistor 90 92, 94, 96, 98, 100, 102, and 104, and a gate and source both connected to V_{SS}. N-channel transistor 106 has a drain connected to the source terminals of all of the parallel-connected N-channel transistors 90, 92, 94, 96, 98, 100, 102, and 104, a gate coupled to a power supply voltage labeled V_{DD}, and source. N-channel transistor 108 has a gate and source connected to VSS, and a drain connected to the source of transistor 106.

A reference cell 110 includes a plurality of series-connected transistors for providing a reference current. Each of the transistors in the plurality of series-connected transistors 110 is electrically equivalent to transistor 26 of array 12. An optional circuit 112 is provided in the

illustrated embodiment to change the number of series-connected transistors used for adjusting the reference current. Each of the switches in option circuit 11 represents metal options in the metal masks to create optional electrical paths for connecting additional reference cells in series. One or more additional transistors can be added using the metal options. If necessary, the number of series-connected transistors can be changed to provide a current that is about half way between the current provided by a selected bit line when the memory cell location is programmed to be a logic "one" or a logic "zero".

A reference bit line labeled BLREF is coupled to reference cell 110. Each of the elements in reference circuit 20 is used to model, or match, the electrical characteristics of a corresponding element of the data path. Reference bit line BLREF includes a bit line that models the impedance of each of the bit lines of memory array 12. The parallel-connected transistors 90, 92, 94, 96, 98, 100, 102, 104 each match the impedance of a decode transistor corresponding to transistor 80 of FIG. 3. Note that there are eight parallel-connected decode transistors in FIG. 4 to correspond to eight decode transistors for coupling eight memory arrays including memory arrays 12 and 14 to precharge and data line decode circuit 22. N-channel transistor 106 is provided to match the impedance of a selected one of decode transistors connecting the BL to DLA such as transistor 32 of FIG. 3 which connects BL<0> to DLA<0>, transistor 34 of FIG. 3 which connects BL<1> to DLA<0>, and other transistors 36, 38, 40, 42, 44, and 46 of FIG. 3 which connect BL<2> through BL<7> to DLA<0>, respectively. Transistor 88 in FIG. 4 matches the impedance of N-channel transistor 82 in FIG 3. Likewise, N-channel transistor 108 is used to match the impedance of the selected one of precharge transistors 48, 50, 52, 54, 56, 58, 60, and 62.

FIG. 5 illustrates, in schematic diagram form, sense amplifier 24 of memory 10 of FIG. 1. Sense amplifier 24 includes cross-coupled latch 114, P-channel transistors 116, 118, 124, and 126, N-channel transistors 120 and 122, and inverters 128, 130, and 132. Cross-coupled latch 114 includes a pair of conventional cross-coupled inverters. P-channel transistors 116 and 118 and N-channel transistors 120 and 122 couple cross-coupled latch 114 to V_{DD1} and V_{SS}, respectively, in response to a logic high sense enable signal SE. Supply voltage V_{DD1} can be different than V_{DD} or the same as V_{DD}. Inverters 128, 130, and 132 are used to invert the logic level of sense enable signal SE to make P-channel transistors 116, 118, 124, and 126 conductive from the logic high sense enable signal SE. Nodes 134 and 136 function as both input and output terminals for cross-coupled latch 114. P-channel transistors 124 and 126 provide current sources for the reference line and the data line during a read cycle.

FIG. 6 illustrates various signals of memory 10 of FIG. 1 useful for understanding a read operation. In FIG. 6, a read cycle for reading a logic "1" from a selected memory location is illustrated between times t0 and t3, and a read cycle for reading a logic "0" from a selected memory location is illustrated between times t3 and t6. To begin a read cycle of memory 10, address signals are decoded to select a word line and a bit line. This is indicated in FIG. 6 at a time between time t0 and time t1 by a logic high word line signal WL and logic high first level column decode signal CPA. When first level column decode signal CPA is asserted, the corresponding precharge transistor becomes substantially non-conductive. All of the other precharge transistors connected to the unselected bit lines continue to couple the unselected bit lines to V_{SS}.

At time t1, second level column decode signal CPB is asserted as a logic high voltage to cause N-channel transistor 80 in FIG. 3 and one of

transistors 90, 92, 94, 96, 98, 100, 102, 104 (FIG. 4) to be conductive. Sense enable signal SE is low causing current source P-channel transistors 124 and 126 to be conductive. P-channel transistors 124 and 126 provide current sources for data DLB and reference line REF, respectively. The effect is to create a current path at time t1 from the selected bit line through data lines DLA<0> and DLB to node 134 of sense amplifier 24. Another current path is created through the reference circuit 20. The data line current and the reference current are the only current paths through memory 10 during the read cycle. As illustrated between times t1 and t2, the data line current causes the voltage labeled DLB"1" to increase faster than the reference line voltage REF because the data line current is larger than the reference current when reading a "1". Note that in the illustrated embodiment, the current through the selected bit line causes the bit line voltage BL to increase from zero to about 600 millivolts (mV) and voltage DLA increases to about 700 mV.

After the data line voltage and reference line voltage have separated from each other by a predetermined amount, sense enable signal becomes a logic high (at time t2), causing P-channel current source transistors 124 and 126 to be substantially non-conductive and causing P-channel transistors 116 and 118 and N-channel transistors 120 and 122 to be conductive, thus allowing the voltage from the selected bit line and the reference line to be provided to cross-coupled latch 114. Also, at time t2, CPB is returned to a logic low, causing the bit line to be decoupled from the data lines and causing the data line DLB precharge transistor 82 to again couple the bit line to V_{SS}. Likewise, after time t2, decode signal CPA returns to a logic low causing the bit line precharge transistor to again couple the bit line to V_{SS}. Between times t2 and t3, the cross-coupled latch 114, resolves with sense amplifier 24 node 134 at a logic high voltage and node 136 at a logic low

voltage. Buffer circuit 28 provides the latched state of sense amplifier 24 as a logic high data out signal DATA OUT corresponding to the stored state of the selected memory location. At time t3, the sense enable signal SE is returned to a logic low causing the voltage of both of nodes 134 and 136 to be increased toward V_{DD1} in preparation for the next read cycle.

Note that in the illustrated embodiment, the column decode signals CPA and CPB are asserted before sense enable signal SE is asserted because some signal differential between DLB and REF must be generated before sense amplifier 24 is enabled. By decoding the precharge voltage applied to the selected bit line and to the reference line, the RC delay can be more accurately matched, thereby providing for faster sensing and better noise margins. By having only one current path during the read cycle, power consumption is reduced.

To begin a read cycle for reading a logic "0" from a selected location of memory 10, address signals are decoded to select a word line and a bit line as indicated in FIG. 6 between times t3 and t4. When first level column decode signal CPA is asserted, the corresponding precharge transistor is substantially non-conductive. All of the other non-selected precharge transistors maintain the unselected bit lines at V_{SS}.

At time t4, second level column decode signal CPB is asserted as a logic high voltage to cause N-channel transistor 80 in FIG. 3 and one of transistors 90, 92, 94, 96, 98, 100, 102, 104 in FIG. 4 to be conductive. Sense enable signal SE is low causing current source P-channel transistors 124 and 126 to be conductive. P-channel transistors 124 and 126 provide current sources for data DLB and reference line REF, respectively. The effect is to create a current path at time t4 from the selected bit line through data lines DLA<0> and DLB to node 134 of sense amplifier 24. Another current path is created through the reference circuit 20. The data line current

and the reference current are the only current paths through memory 10 during the read cycle. As illustrated between times t4 and t5, the data line current causes the voltage labeled DLB"0" to increase slower than the reference line voltage REF because the data line current is lower than the reference line current when reading a "0". In the illustrated embodiment, voltage BL will increase from zero volts to about 400 mV and voltage DLA increases from zero volts to about 500 mV.

At time t5, sense enable signal becomes a logic high, causing P-channel transistors 124 and 126 to be substantially non-conductive and causing P-channel transistors 116 and 118 and N-channel transistors 120 and 122 to be conductive, thus allowing the voltage from the selected bit line and the reference line to be provided to cross-coupled latch 114. At time t4, the voltage on data line DLB and the reference line REF began to separate. The state sensed by sense amplifier 24 is determined by whether there is a transistor at the selected bit line location. To read a zero, there must be a transistor located at the selected memory cell location to provide a greater current than the reference current provided by reference cell 110. At time t5, CPB is returned to a logic low, causing the bit line to be decoupled from the data lines and causing the precharge transistor to again couple the bit line to V_{SS}. As illustrated in FIG. 6, the voltage on reference line REF is increasing faster, indicating that the selected memory cell location has a transistor to sink more current. Between times t5 and t6, the cross-coupled latch 114, resolves with node 134 at a logic low voltage and node 136 at a logic high voltage and buffer circuit 28 provides the latched state as data out signal DATA OUT. At time t6, the sense enable signal SE is returned to a logic low causing the voltage of both of nodes 134 and 136 to be increased toward V_{DD1} in preparation for the next read cycle.

Although the invention has been described with respect to specific memory devices, those of ordinary skill in the art will appreciate that the invention may also be used in connection with other memory devices such as, for example, thyrister random access memory (TRAM), programmable read only memory (PROM), electrically programmable read only memory (EPROM), flash memory, magnetic random access memory (MRAM), microprocessors containing cache memory, and the like.

While the invention has been described in the context of a preferred embodiment, it will be apparent to those skilled in the art that the present invention may be modified in numerous ways and may assume many embodiments other than that specifically set out and described above. Accordingly, it is intended by the appended claims to cover all modifications of the invention which fall within the true scope of the invention.

Benefits, other advantages, and solutions to problems have been described above with regard to specific embodiments. However, the benefits, advantages, solutions to problems, and any element(s) that may cause any benefit, advantage, or solution to occur or become more pronounced are not to be construed as a critical, required, or essential feature or element of any or all the claims. As used herein, the terms "comprises," "comprising," or any other variation thereof, are intended to cover a non-exclusive inclusion, such that a process, method, article, or apparatus that comprises a list of elements does not include only those elements but may include other elements not expressly listed or inherent to such process, method, article, or apparatus.

CLAIMS

What is claimed is:

1. A method for reading a memory device, the method comprising the steps of:

precharging a bit line of the memory device;

selecting a memory cell on the bit line to read, the memory cell having a circuit characteristic of either a first state or a second state indicative of a first value stored in the memory cell or a second value stored in the memory cell, respectively;

concurrently driving a first current through a data path including the bit line to charge the data path and driving a second current through a reference circuit, the reference circuit including a reference cell having a circuit characteristic located between the first state and the second state; and

comparing a voltage resulting from the driving of the first current through the data path with a voltage resulting from the driving of the second current through the reference circuit to determine whether the first value or the second value is stored in the memory cell, wherein the voltage resulting from the driving of the first current through the data path is dependent upon the circuit characteristic.

2. The method of claim 1 wherein the step of concurrently driving further includes:

providing a decode signal to a decode switch in the data path to electrically couple the bit line to a first current source and providing the decode signal to a reference switch of the

reference circuit to electrically couple the reference cell to a second current source.

3. The method of claim 2 wherein the step of selecting further comprises:
providing another decode signal to another decode switch in the data path to electrically couple the bit line to the decode switch.

4. The method of claim 1 wherein the circuit characteristic includes a resistance between the bit line and a voltage source when the memory cell is selected, wherein the first state includes a first level of resistance between the bit line and the voltage source, wherein the second state includes a second level of resistance between the bit line and the voltage source, wherein the reference characteristic is a resistance level between the first resistance level and the second resistance level.

5. The method of claim 1 further comprising the step of:
coupling the decode signal to a precharge circuit, the precharge circuit for precharging a bit line to a predetermined voltage prior to a read access, the decode signal for causing the precharge circuit to be decoupled from the bit line during the read access.

6. The method of claim 1 wherein the step of precharging a bit line further includes precharging a plurality of bit lines including the bit line, each of the plurality of bit lines selectively coupleable to a current source via a data line, the method further comprising the step of:
precharging the plurality of the bit lines other than the bit line during the step of concurrently driving current.

7. The method of claim 1 wherein the reference circuit further includes a reference bit line electrically coupled to the reference cell.

8. A memory device comprising:

a plurality of memory cells, each of the memory cells having a circuit characteristic of either a first state or a second state indicative of a first value stored in the memory cell or a second value stored in the memory cell, respectively;

a bit line electrically connected to at least one memory cell of the plurality of memory cells;

a reference circuit including a reference cell and a reference switch having a control input;

a data line;

a decode switch for electrically coupling the data line to the bit line, the decode switch having a control input;

wherein the control input of the decode switch and the control input of the reference switch are electrically coupled to receive a decode signal, wherein during a memory cell read, the decode signal closing the decode switch to drive a current through the bit line and a memory cell of the plurality of memory cells to be read and closing the reference switch to drive a reference current through the reference circuit;

an output circuit configured to provide a data signal indicative of a value stored in a memory cell of the plurality of memory cells as by comparing a voltage resulting from driving the current though the bit line and the memory cell and a voltage resulting from driving the reference current through the reference circuit.

9. The memory device of claim 8 further comprising:

a precharge circuit electrically coupled to the data line, the precharge circuit including a control input electrically coupled to receive the decode signal, wherein during a read cycle, the decode signal decoupling the data line from the precharge circuit.

10. The memory device of claim 8 further comprising:

another decode switch electrically coupled to the bit line and electrically coupled to the decode switch, the other decode switch being controlled by an other decode signal, wherein during the memory cell read, the decode switch is closed during a driving of current through the bit line and the memory cell to be read.

11. The memory device of claim 10 further comprising:

a precharge circuit electrically coupled to the bit line and being controlled by the other decode signal, the precharge circuit is decoupled from the bit line during a driving of current through the bit line during the memory cell read.

12. The memory device of claim 8 wherein the memory cell of the plurality of memory cells is a read only memory (ROM) cell, and wherein when a memory cell of the plurality of memory cells has a circuit characteristic of the first state, the memory cell includes a transistor having one terminal electrically connected to a bit line, a second terminal electrically connected to a voltage source, and a control terminal electrically connected to a word line of the memory device, wherein when a memory cell has a circuit characteristic of the second state, the memory cell does not include a transistor.

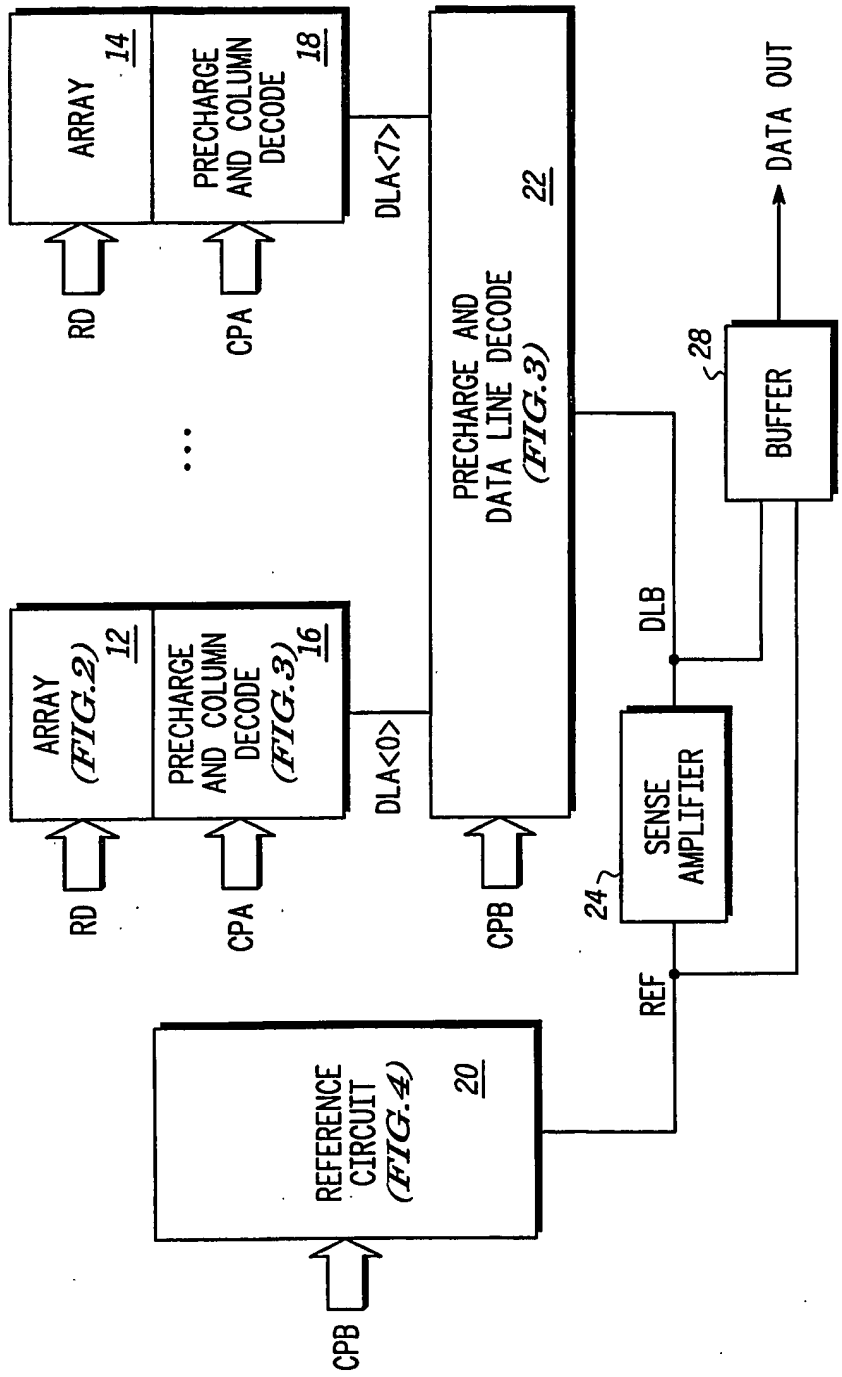
13. The memory device of claim 8 further comprising:

a plurality of decode switches including the decode switch, each of the plurality of decode switches including a control input for receiving one of a plurality of decode signals including the decode signal, the plurality of decode switches being of a first number;

a plurality of reference switches including the reference switch, each of the plurality of reference switches including a control input for receiving one of the decode signals of the plurality of decode signals, each of the plurality of reference switches includes a first side electrically coupled to the reference cell, the plurality of reference switches being of the first number;

wherein during the memory cell read, a decode signal of the plurality of decode signals closes a decode switch of the plurality of decode switches to drive current through a bit line and the memory cell and closes a reference switch of the plurality to drive current through the reference circuit.

14. The memory device of claim 8 wherein the reference circuit further includes a reference bit line electrically coupled to the reference cell.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PRECHARGE AND COLUMN DECODE
18
RD
CPA
DLA<7>
PRECHARGE AND DATA LINE DECODE (FIG.3)
22
DATA OUT
28
BUFFER
ARRAY (FIG.2)
12
PRECHARGE AND COLUMN DECODE (FIG.3)
16
DLA<0>
DLB
SENSE AMPLIFIER
24
CPB
REF
REFERENCE CIRCUIT (FIG.4)
20
10

FIG.1

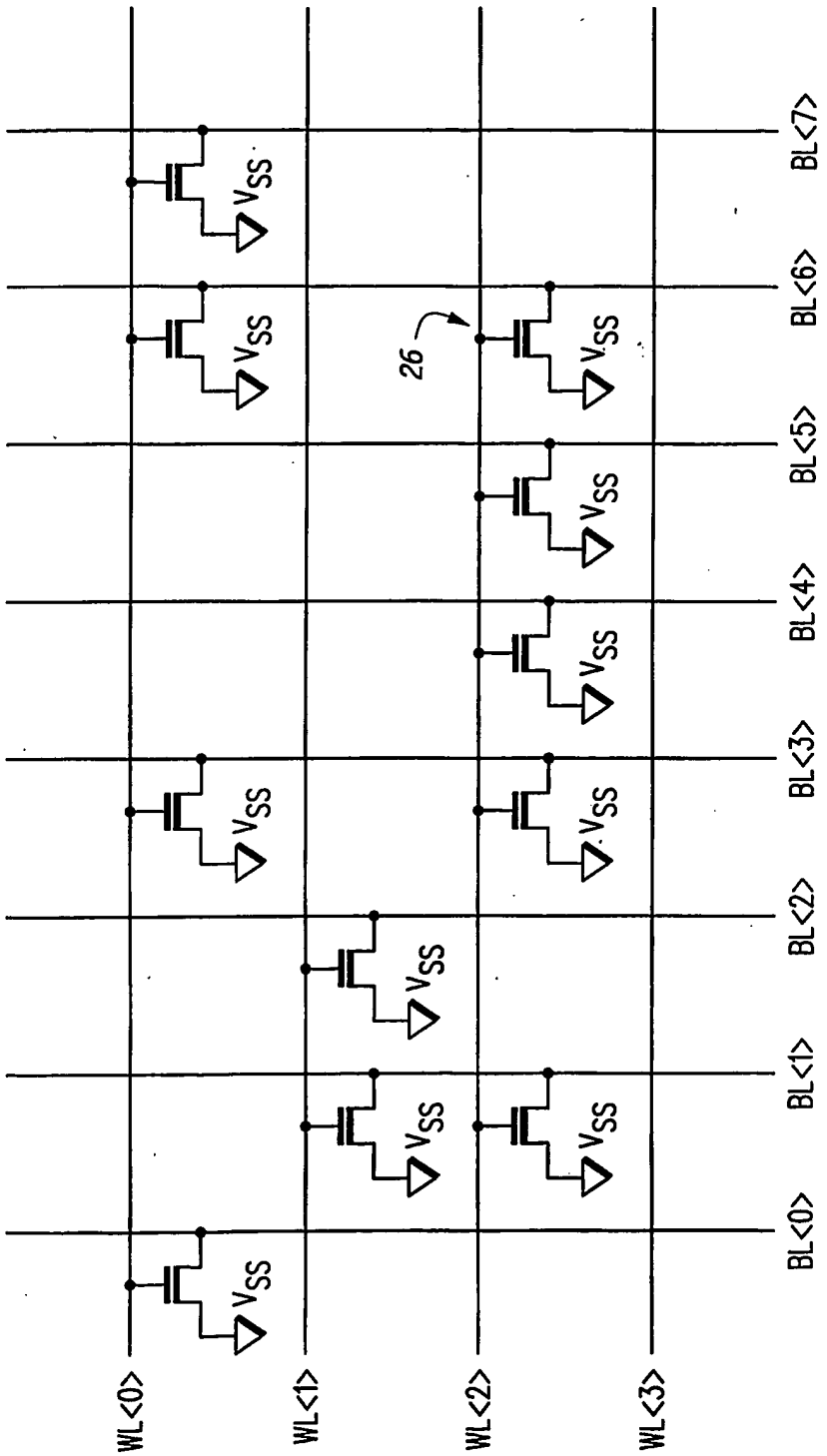
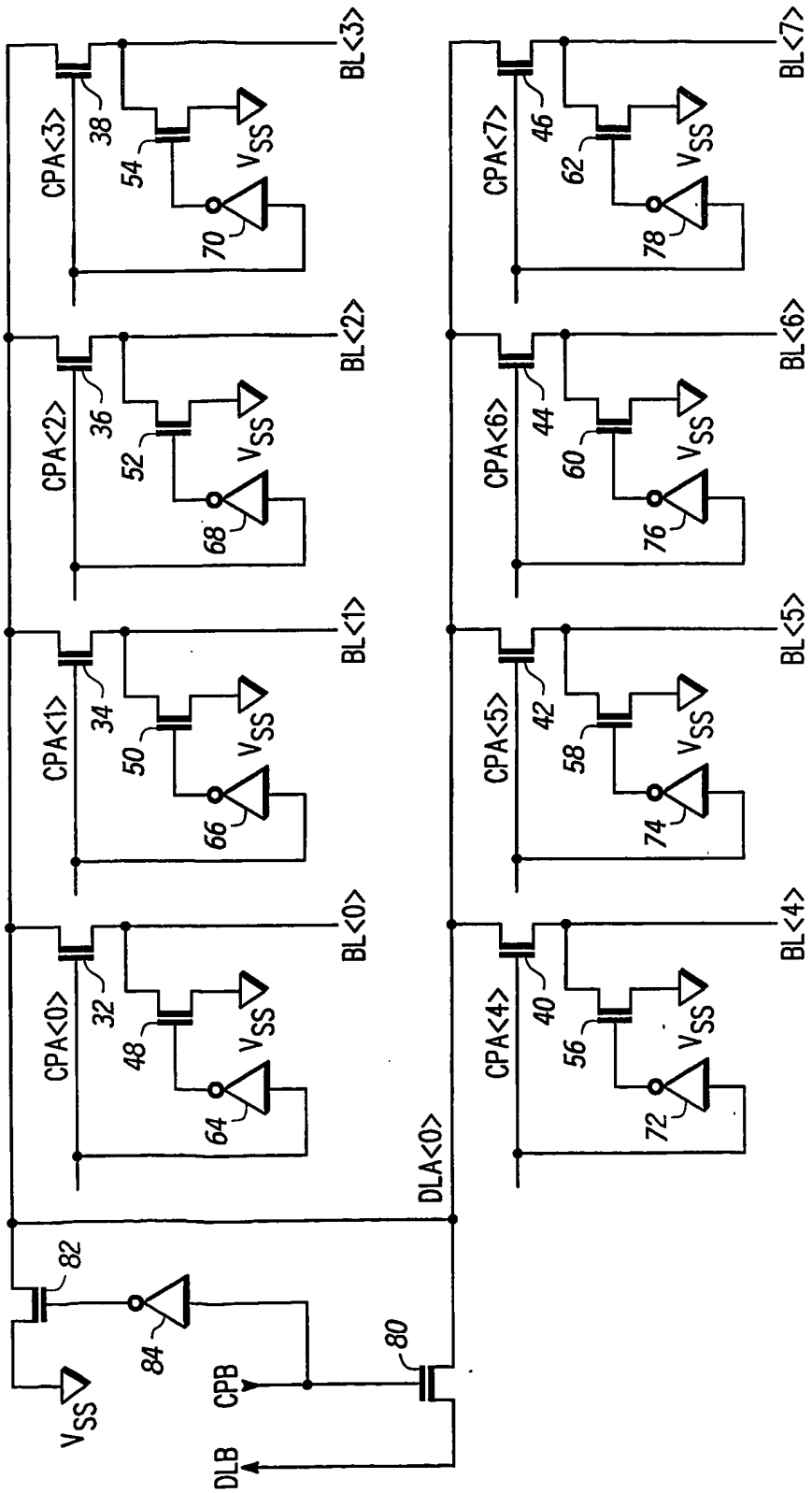


FIG.2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68
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64
78
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74
72
V_{SS}
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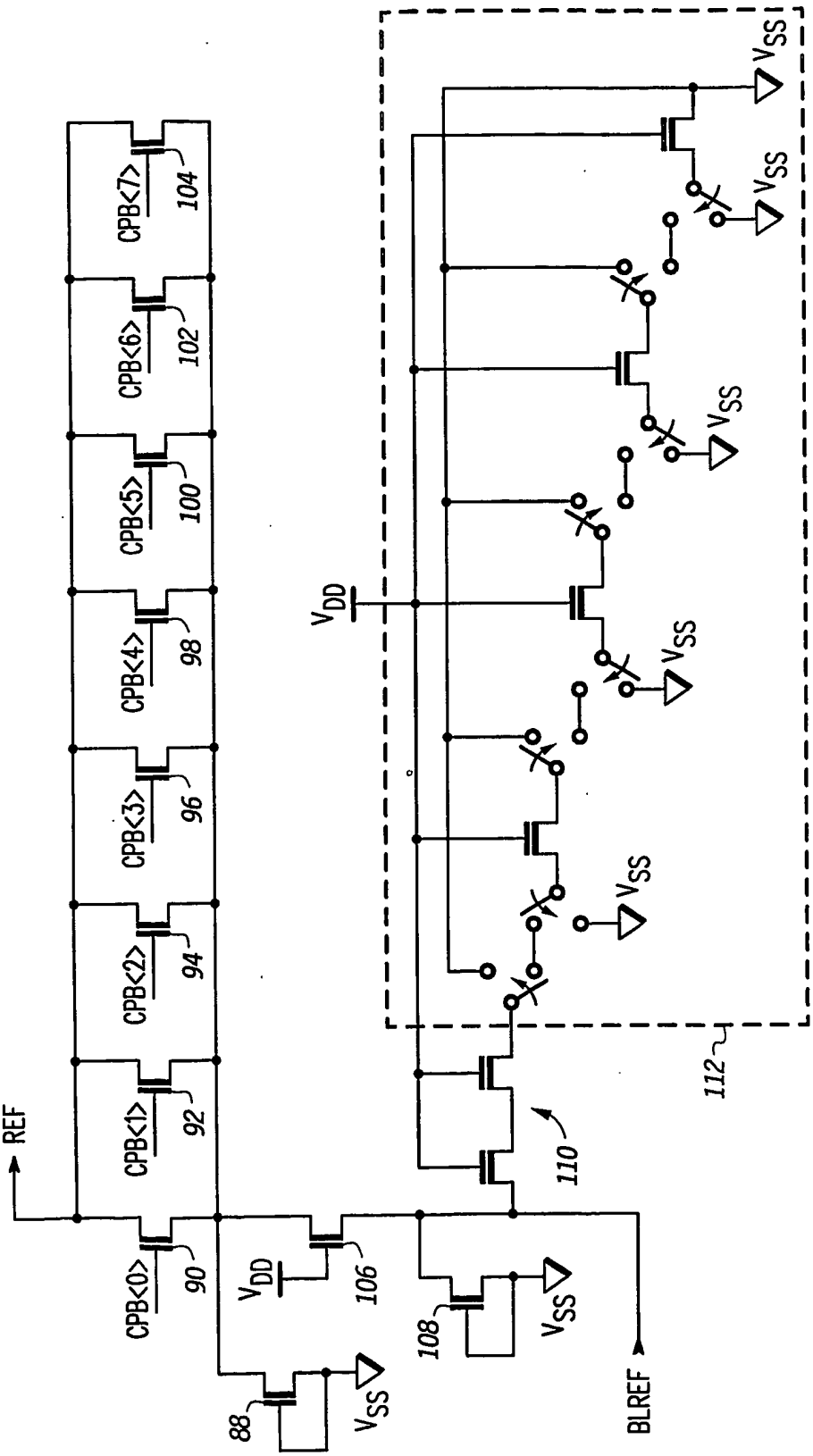
82
84
80
CPB
DLB
30

FIG.3


REF
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CPB<1>
CPB<2>
CPB<3>
CPB<4>
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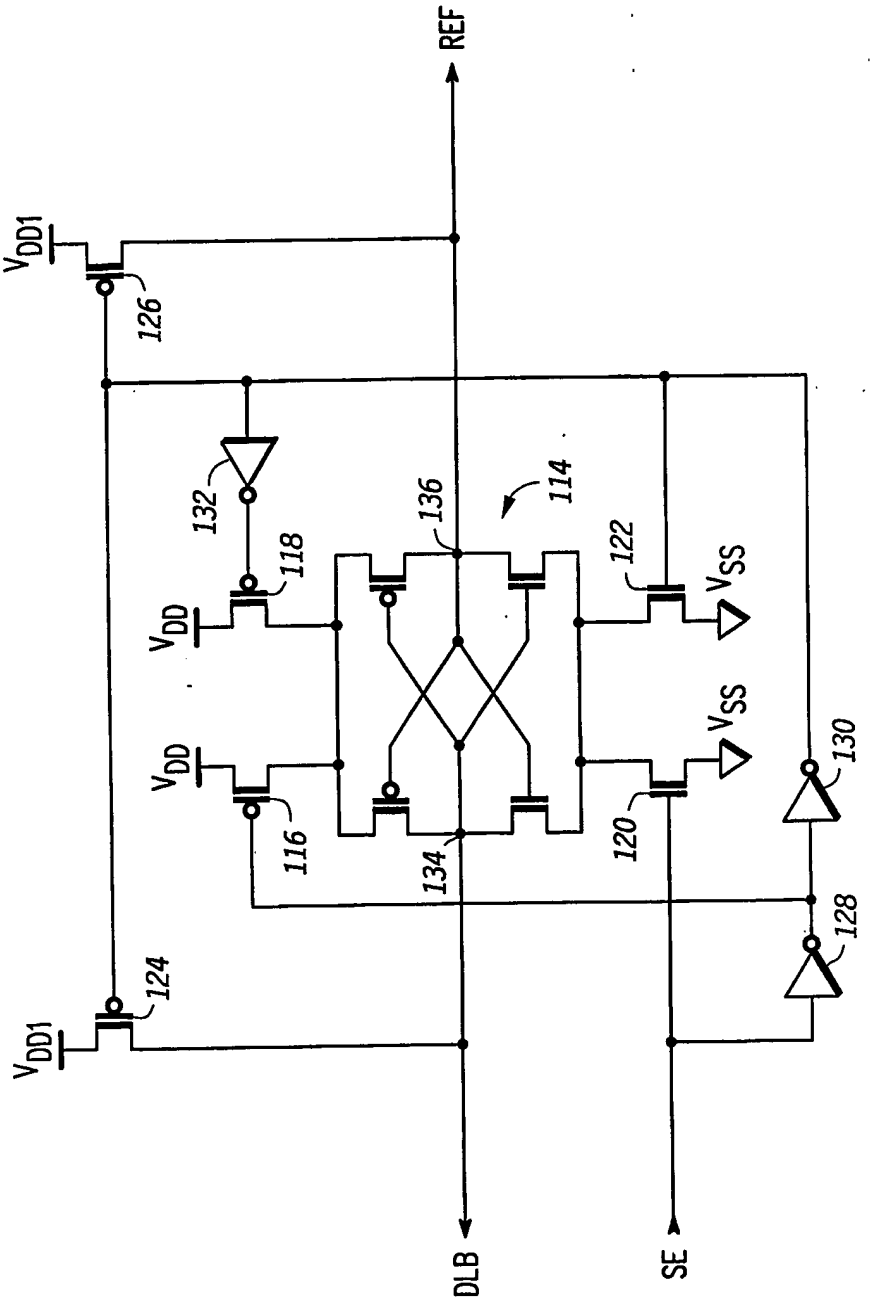
CPB<6>
CPB<7>
90
92
94
96
98
100
102
104
88
106
108
110
112
20
V_{DD}
V_{SS}
BLREF

FIG. 4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V_{DD1}
126
132
118
136
114
122
V_{SS}
V_{DD}
V_{SS}
130
V_{DD}
116
134
120
128
124
V_{DD1}
DLB
SE
24

FIG.5

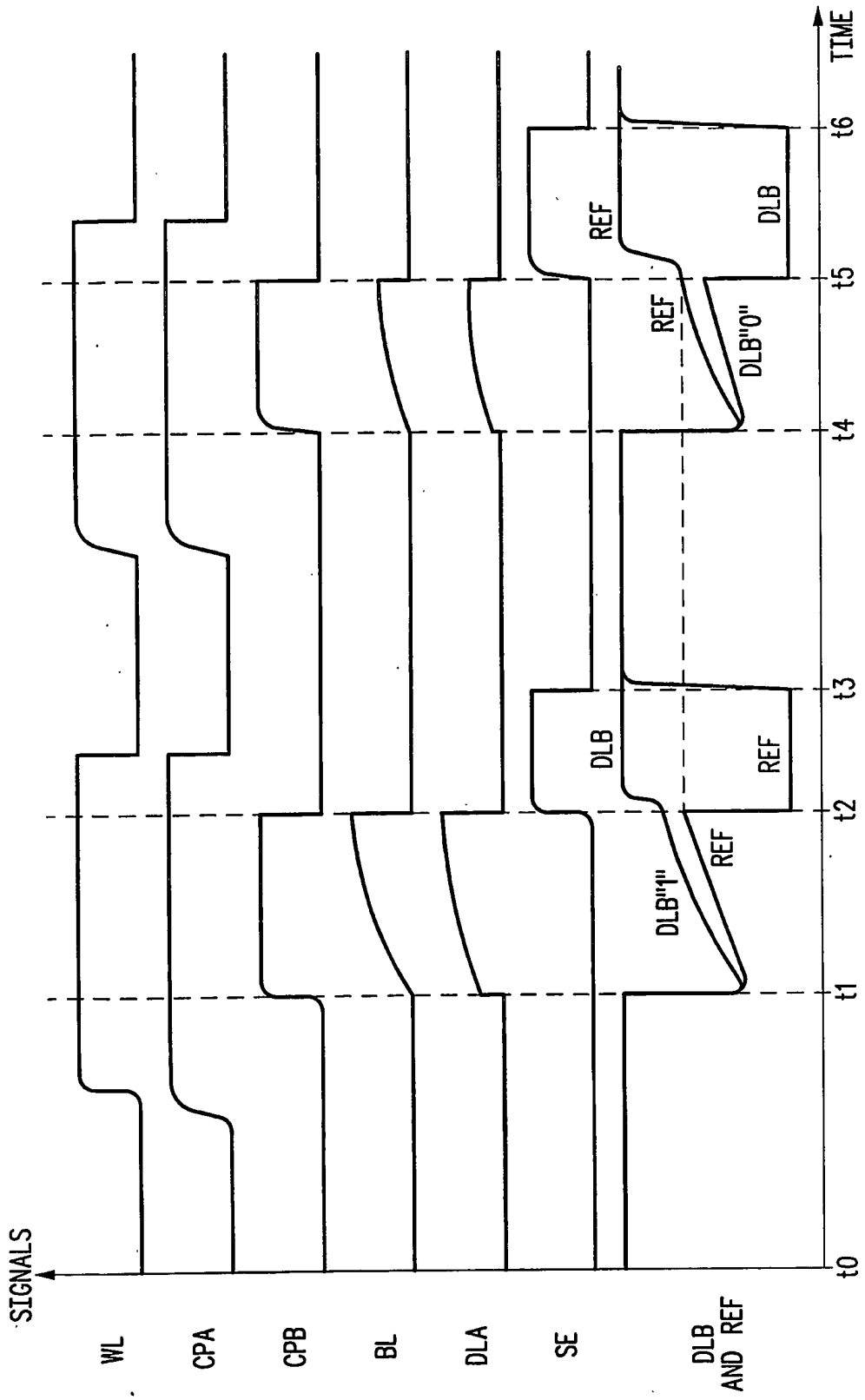
SIGNALS
WL
CPA
CPB
BL
DLA
SE
DLB AND REF
t0
t1
t2
t3
t4
t5
t6
TIME
DLB
REF
DLB"1"
REF
DLB
REF
DLB"0"
REF
DLB

FIG.6

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US02/25617

A. CLASSIFICATION OF SUBJECT MATTER
IPC(7) : G11C 17/00
US CL : 365/104
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 365/104, 189.07, 203, 204, 205

Documentation searched other than minimum documentation to the extent that such documents are included in the fields search

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EAST

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim N
X	US 5,703,820 A (KOHMO) 30 December 1997 (30.12.1997), column 4, line 16 to column 5, line 45 and figure 2.	1-24
A	US 5,745,401A (LEE) 28 April 1998 (28.4.1998), column 1, lines 35-43 and figure 1C.	

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
24 September 2002 (24.09.2002)	17 DEC 2002
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703)305-3230	Authorized officer Hoai V. Ho Telephone No. (703) 308-0956

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